## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of performing a fast information compare within a processor comprising:

performing a ~~more significant bit compare~~ first comparison when a first information is loaded into a translation lookaside buffer, ~~the more significant bit compare~~ comparing bits corresponding to a page number ~~more significant bits~~ of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number ~~more significant bits~~ of a compare information;

storing a result of the ~~more significant bit compare~~ first comparison within the translation lookaside buffer as part of an entry ~~containing~~ corresponding to the first information; and

using the stored result ~~of the more significant bit compare~~ in conjunction with ~~results from a compare of less significant bits~~ a second comparison comparing bits corresponding to a page offset of ~~the~~ a second information and ~~less significant~~ bits corresponding to a page offset of the compare information to determine whether a match is present between the second information and the compare information.

2. (Currently Amended) The method of claim 1 further comprising:

providing an indication of a match to the compare information when the stored result ~~of the more significant bit compare~~ is active and the ~~less significant~~ bits corresponding to a page offset of the second information match the ~~less significant~~ bits corresponding to a page offset of the compare information.

3. (Currently Amended) The method of claim 1 wherein:

the compare information corresponds to a virtual address watchpoint~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address~~.

4. (Currently Amended) The method of claim 1 wherein:

the compare information corresponds to a sample selection criteria~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria~~.

5. (Currently Amended) The method of claim 4 wherein:

the sample selection criteria includes a ~~sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address~~ first address and a second address corresponding to an address range; and

the result of the ~~more significant bit compare~~ first comparison indicates whether the ~~more significant~~ bits corresponding to a page number of the first information being loaded correspond to one of a plurality of conditions ~~indicated by the sample selection criteria~~ indicating whether a page corresponding to the first information is entirely inside the range, entirely outside the range, includes the entire range, includes the first address and includes the second address.

6. (Currently Amended) The method of claim 1 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the ~~more significant bit compare~~ first comparison is performed when the first information is loaded into the instruction translation lookaside buffer.

7. (Currently Amended) The method of claim 1 wherein:

the processor includes a plurality of threads; and

the compare information ~~is unique for each of~~ corresponds to one of the plurality of threads.

8. (Currently Amended) An apparatus for performing a fast information compare within a processor comprising:

means for performing a ~~more significant bit compare~~ first comparison when a first information is loaded into a translation lookaside buffer, ~~the more significant bit compare~~ comparing bits corresponding to a page number ~~more significant bits~~ of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number ~~more significant bits~~ of a compare information;

means for storing a result of the ~~more significant bit compare~~ first comparison within the translation lookaside buffer as part of an entry ~~containing~~ corresponding to the first information; and

means for using the stored result ~~of the more significant bit compare~~ in conjunction with ~~results from a compare of less significant bits~~ a second comparison comparing bits corresponding to a page offset of ~~the~~ a second information and ~~less significant~~ bits corresponding to a page offset of the compare information to determine whether a match is present between the second information and the compare information.

9. (Currently Amended) The apparatus of claim 8 further comprising:

means for providing an indication of a match to the compare information when the stored result ~~of the more significant bit compare~~ is active and the ~~less significant~~ bits corresponding to a page offset of the second information match the ~~less significant~~ bits corresponding to a page offset of the compare information.

10. (Currently Amended) The apparatus of claim 8 wherein:

the compare information corresponds to a virtual address watchpoint~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address~~.

11. (Currently Amended) The apparatus of claim 8 wherein:

the compare information corresponds to a sample selection criteria~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria~~.

12. (Currently Amended) The apparatus of claim 11 wherein:

the sample selection criteria includes a ~~sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address~~ first address and a second address corresponding to an address range; and

the result of the ~~more significant bit compare~~ first comparison indicates whether the ~~more significant~~ bits corresponding to a page number of the first information being loaded correspond to one of a plurality of conditions ~~indicated by the sample selection criteria~~ indicating whether a page corresponding to the first information is entirely inside the range, entirely outside the range, includes the entire range, includes the first address and includes the second address.

13. (Currently Amended) The apparatus of claim 8 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the ~~more significant bit compare~~ first comparison is performed when the first information is loaded into the instruction translation lookaside buffer.

14. (Currently Amended) The apparatus of claim 8 wherein:

the processor includes a plurality of threads; and

the compare information ~~is unique for each of~~ corresponds to one of the plurality of threads.

15. (Currently Amended) A processor comprising:

a translation lookaside buffer; and

a first compare unit coupled to the translation lookaside buffer, the first compare unit performing a ~~more significant bit compare~~ first comparison when a first information is loaded into a translation lookaside buffer, ~~the more significant bit compare~~ comparing bits corresponding to a page number ~~more significant bits~~ of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number ~~more significant bits~~ of a compare information, the ~~first compare unit~~ the translation lookaside buffer storing a result of the ~~more significant bit compare~~ first comparison within the translation lookaside buffer as part of an entry ~~containing~~ corresponding to the first information; and

a second compare unit coupled to the translation lookaside buffer, the second compare unit ~~processor~~ using the stored result ~~of the more significant bit compare~~ in conjunction with ~~results from a compare of less significant bits~~ a second comparison comparing bits corresponding to a page offset of ~~the~~ a second information and ~~less significant~~ bits corresponding to a page offset bits of the compare information to determine whether a match is present between the second information and the compare information.

16. (Currently Amended) The processor of claim 15 wherein:

the second compare unit provides an indication of a match to the compare information when the stored result ~~of the more significant bit compare~~ is active and the ~~less significant~~ bits corresponding to a page offset of the second information match the ~~less significant~~ bits corresponding to a page offset of the compare information.

17. (Currently Amended) The processor of claim 15 wherein:

the compare information corresponds to a virtual address watchpoint~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address~~.

18. (Currently Amended) The processor of claim 15 wherein:

the compare information corresponds to a sample selection criteria~~; and~~

~~the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria~~.

19. (Currently Amended) The processor of claim 18 wherein:

the sample selection criteria includes a ~~sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address~~ first address and a second address corresponding to an address range; and

the result of the ~~more significant bit compare~~ first comparison indicates whether the ~~more significant~~ bits corresponding to a page number of the first information being loaded correspond to one of a plurality of conditions ~~indicated by the sample selection criteria~~ indicating whether a page corresponding to the first information is entirely inside the range, entirely outside the range, includes the entire range, includes the first address and includes the second address.

20. (Currently Amended) The processor of claim 15, further comprising:

a memory management unit, the memory management unit including a memory management unit translation lookaside buffer; and

an instruction fetch unit, the instruction fetch unit including an instruction translation lookaside buffer, the ~~more significant bit compare~~ first comparison being performed when the first information is loaded into the instruction translation lookaside buffer.

21. (Currently Amended) The processor of claim 15 wherein:

the processor includes a plurality of threads; and

the compare information ~~is unique for each of~~ corresponds to one of the plurality of threads.